Modulbezeichnung:	**Reconfigurable Computing (RC)**	**7.5 ECTS**
Modulverantwortliche/r:	Jürgen Teich	
Lehrende:	Daniel Ziener, Jürgen Teich	

Startsemester: WS 2011/2012	Dauer: 1 semester	
Präsenzzeit: 90 Std.	Eigenstudium: 135 Std.	Sprache:

Lehrveranstaltungen:

Im Rahmen des Moduls sind Vorlesung und Übung zu Reconfigurable Computing verpflichtend. Optional kann das Praktikum Reconfigurable Computing besucht werden. Dies ermöglicht die Erhöhung der angerechneten Punkte von 5 auf 7.5 ECTS.

Reconfigurable Computing (WS 2011/2012, Vorlesung, 2 SWS, Jürgen Teich et al.)
Exercises to Reconfigurable Computing (WS 2011/2012, Übung, 2 SWS, Srinivas Boppu)
Praktikum Reconfigurable Computing (WS 2011/2012, optional, Praktikum, Tobias Ziermann)

Inhalt:

Reconfigurable (adaptive) computing is a novel yet important research field investigating the capability of hardware to adapt to changing computational requirements such as emerging standards, late design changes, and even to changing processing requirements arising at run-time. Reconfigurable computing thus benefits from a) the programmability of software similar to the Von Neumann computer and b) the speed and efficiency of parallel hardware execution.

The purpose of the course reconfigurable computing is to instruct students about the possibilities and rapidly growing interest in adaptive hardware and corresponding design techniques by providing them the necessary knowledge for understanding and designing reconfigurable hardware systems and studying applications benefiting from dynamic hardware reconfiguration.

Lernziele und Kompetenzen:

After a general introduction about benefits and application ranges of reconfigurable (adaptive) computing in contrast to general-purpose and application-specific computing, the following topics will be covered:

- Reconfigurable computing systems: Introduction of available technology including fine grained look up table (LUT-) based reconfigurable systems such as field programmable gate arrays (FPGA) as well as newest coarse grained architectures and technology.
- Design and implementation: Algorithms and steps (design entry, functional simulation, logic synthesis, technology mapping, place and route, bit stream generation) to implement (map) algorithms to FPGAs. The main focus lies on logic synthesis algorithms for FPGAs, in particular LUT technology mapping.
- Temporal partitioning: techniques to reconfigure systems over time. Covered are the problems of mapping large circuits which do not fit one single device. Several temporal partitioning techniques are studied and compared.
- Temporal placement: Techniques and algorithms to exploit the possibility of partial and dynamic (run-time) hardware reconfiguration. Here, OS-like services are needed that optimize the allocation and scheduling of modules at run-time.
- On-line communication: Modules dynamically placed at run-time on a given device need to communicate as well as transport data off-chip. State-of-the-art techniques are introduced how modules can communicate data at run-time including bus-oriented as well as network-on-a-chip (NoC) approaches.
- Designing reconfigurable applications on Xilinx Virtex FPGAs: In this part, the generation of partial bitstreams for components to be placed at run-time on Xilinx FPGAs is introduced and discussed including newest available tool flows.
- Applications: This section presents applications benefiting from dynamic hardware reconfiguration. It covers the use of reconfigurable systems including rapid prototyping, reconfigurable supercomputers, reconfigurable massively parallel computers and studies important application domains such as distributed arithmetic, signal processing, network packet processing, control design, and cryptography.

Literatur:

- The Hamburg VHDL Archive (see Documentation link for free books)
- Interactive VHDL Tutorial with 150 examples from ALDEC
- Easy FPGA tutorials, projects and boards
- Xilinx WebPack ISE and Modelsim MXE (free FPGA synthesis tool and free VHDL simulator)
- Symphone EDA free VHDL simulator (select FREE Edition license)
- Icarus open-source Verilog simulator

Verwendbarkeit des Moduls / Einpassung in den Musterstudienplan:

Das Modul ist im Kontext der folgenden Studienfächer/Vertiefungsrichtungen verwendbar:

[1] **Informatik (Bachelor of Science)**
(Po-Vers. 2009s | Praktika und Wahlpflichtbereich (5. und 6. Semester) | Wahlpflichtmodule | Vertiefungsmodul Hardware-Software-Co-Design)

[2] **Informatik (Bachelor of Science)**
(Po-Vers. 2009w | Praktika und Wahlpflichtbereich (5. und 6. Semester) | Wahlpflichtmodule | Vertiefungsmodul Hardware-Software-Co-Design)

[3] **Informatik (Master of Science)**
(Po-Vers. 2010 | Wahlpflichtbereich | Säule der systemorientierten Vertiefungsrichtungen | Vertiefungsmodul Hardware-Software-Co-Design)

[4] **Informations- und Kommunikationstechnik (Master of Science)**
(Po-Vers. 2010 | Schwerpunkt Eingebettete Systeme | Wahlpflichtmodule | Wahlpflichtmodul aus INF im Schwerpunkt Eingebettete Systeme)

[5] **Informations- und Kommunikationstechnik (Master of Science)**
(Po-Vers. 2010 | Schwerpunkt Realisierung von Informations- und Kommunikationssystemen | Wahlpflichtmodule | Wahlpflichtmodul aus INF im Schwerpunkt Realisierung von Informations- und Kommunikationssystemen)

Studien-/Prüfungsleistungen:

Reconfigurable Computing (Vorlesung mit Übung)
(diese Prüfung gilt nur im Kontext der Studienfächer/Vertiefungsrichtungen [1], [2], [3])
Studienleistung

Erstablegung: WS 2011/2012, 1. Wdh.: SS 2012
1. Prüfer: Jürgen Teich

Reconfigurable Computing (Vorlesung mit Übung und Praktikum)
(diese Prüfung gilt nur im Kontext der Studienfächer/Vertiefungsrichtungen [1], [2], [3])
Studienleistung

Erstablegung: WS 2011/2012, 1. Wdh.: SS 2012
1. Prüfer: Jürgen Teich

Reconfigurable Computing (Vorlesung mit Übung)
(diese Prüfung gilt nur im Kontext der Studienfächer/Vertiefungsrichtungen [4], [5])
schriftlich, Dauer (in Minuten): 90

Erstablegung: WS 2011/2012, 1. Wdh.: SS 2012
1. Prüfer: Jürgen Teich

Reconfigurable Computing (Vorlesung mit Übung und Praktikum)
(diese Prüfung gilt nur im Kontext der Studienfächer/Vertiefungsrichtungen [4], [5])
schriftlich, Dauer (in Minuten): 90

Erstablegung: WS 2011/2012, 1. Wdh.: SS 2012, 2. Wdh.: WS 2012/2013
1. Prüfer: Jürgen Teich

Bemerkungen:

Reconfigurable computing is an interdisciplinary field of research between computer science and electrical engineering on a 4 SWS (4 hours/week) basis. Lecture and Exercises will give 5 ECTS, the FPGA & VHDL labs 2.5 ECTS.